AMENDMENTS TO THE CLAIMS

Please cancel claims 13 and 16 without prejudice. Please add new claims 22-24.

1. (CURRENTLY AMENDED) An apparatus comprising:

a processor (i) configured to operate at a first data rate in response to a first clock signal and (ii) having a first bus interface unit to communicate on a system bus;

an interface circuit having (A) a state machine, ~~and~~ (B) a second bus interface unit to communicate on said system bus and (C) a control status register having a completion bit that indicates in alternate states that (a) said processor is finished with a current transfer to said interface circuit and (b) said interface circuit is ready to begin a new operation, said interface circuit being configured to (i) operate at a second data rate in response to a second clock signal and (ii) convert data received from said processor over said system bus from said first data rate to said second data rate; and

a first memory (i) having a plurality of banks, (ii) coupled to said interface circuit and (iii) configured to present/receive said data to/from said interface circuit at said second data rate, wherein said state machine is configured to

precharge and close all of said banks prior to a refresh cycle being performed.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first clock signal and said second clock signal are independently generated.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second clock signal is generated in response to said first clock signal.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein state machine is configured to control the conversion between said first data rate and said second data rate.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said apparatus provides paging to said first memory.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said processor comprises (i) a central processing unit (CPU) and a memory control unit that communicates with a second memory.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said interface circuit further comprises a bi-directional first-in-first-out buffer configured to transfer said data between said second bus interface unit and said state machine.

8. (CANCELED)

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said interface circuit is configured to minimize access requests to said first memory.

10. (CURRENTLY AMENDED) An apparatus comprising:

processor means for (i) operating at a first data rate in response to a first clock signal and (ii) having a first bus interface unit to communicate on a system bus;

interface means having (A) a state machine, ~~and~~ (B) a second bus interface unit to communicate on said system bus and (C) a control status register having a completion bit that indicates in alternate states that (a) said processor means is finished with a current transfer to said interface means and (b) said interface means is ready to begin a new operation, said interface means configured for (i) operating at a second data rate in response to a second clock signal, and (ii) converting data received from said

processor means over said system bus from said first data rate to said second data rate; and

memory means (i) having a plurality of banks, (ii) coupled to said interface means and (iii) presenting said data to/from ~~said~~ said interface means at said second data rate, wherein said state machine is configured to precharge and close all of said plurality of banks prior to a refresh cycle being performed.

11. (CURRENTLY AMENDED) A method for paging to a memory comprising the steps of:

(A) operating a processor at a first data rate in response to a first clock signal, said processor communicating on a system bus through a first bus interface unit;

(B) operating an interface circuit at a second data rate in response to a second clock signal, said interface circuit communicating on said system bus through a second bus interface unit and said interface circuit comprising a control status register having a completion bit that indicates in alternate states that (i) said processor is finished with a current transfer to said interface circuit and (ii) said interface circuit is ready to begin a new operation;

(C) converting data received from said processor over said system bus from said first data rate to said second data rate in said interface circuit;

(D) operating said memory (i) having a plurality of banks, (ii) coupled to said interface circuit and (iii) presenting/receiving said data to/from said interface circuit at said second data rate; and

(E) precharging and closing all of said plurality of banks prior to a refresh cycle being performed.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said processor includes a direct memory access engine and said apparatus provides a delay when said direct memory access engine is not ready to present/receive said data to/from said first memory during a read/write operation.

13. (CANCELED)

14. (CURRENTLY AMENDED) The apparatus according to claim ~~13~~ 12, wherein said apparatus is ready to begin said new read/write operation to/from said first memory when said completion bit is cleared.

15. (CURRENTLY AMENDED) The apparatus according to claim ~~14~~ 1, further comprising ~~wherein~~ a direct memory access engine having an upper bound register that is set in response to said completion bit being cleared.

16. (CANCELLED)

17. (CURRENTLY AMENDED) The apparatus according to claim ~~16~~ 15, wherein said direct memory access engine is configured to perform (i) a write operation when ~~said direct memory access~~ a lower bound register is clear and (ii) a read operation when said ~~direct memory access~~ lower bound register is set.

18. (PREVIOUSLY PRESENTED) The apparatus according to claim 17, wherein said direct memory access engine is configured to present an interrupt signal to said processor in response to completing a block of transfer during the read/write operation.

19. (PREVIOUSLY PRESENTED) The apparatus according to claim 18, wherein said processor is configured to determine if more blocks are needed to be transferred during the read/write operation.

20. (PREVIOUSLY PRESENTED) The apparatus according to claim 19, wherein said completion bit is set if there are no more blocks needed to be transferred during the read/write operation.

21. (CURRENTLY AMENDED) The apparatus according to claim ~~13~~ 1, wherein said control status register includes a direction bit

configured to indicate (i) a write operation when said direction bit is clear and (ii) a read operation when said direction bit is set.

22. (NEW) An apparatus comprising:

a processor (i) configured to operate at a first data rate in response to a first clock signal and (ii) having a first bus interface unit to communicate on a system bus;

an interface circuit having (A) a state machine and (B) a second bus interface unit to communicate on said system bus, said interface circuit being configured to (i) operate at a second data rate in response to a second clock signal and (ii) convert data received from said processor over said system bus from said first data rate to said second data rate; and

a first memory (i) having a plurality of banks,(ii) coupled to said interface circuit and (iii) configured to present/receive said data to/from said interface circuit at said second data rate, wherein said state machine is configured to precharge and close all of said banks prior to a refresh cycle being performed,

wherein (A) said processor includes a direct memory access engine and said apparatus provides a delay when said direct memory access engine is not ready to present/receive said data to/from said first memory during a read/write operation, (B) said

interface circuit comprises a control status register having a completion bit which indicates that said apparatus is ready to begin a new read/write operation, (C) said apparatus is ready to begin said new read/write operation to/from said first memory when said completion bit is cleared and (D) a direct memory access upper bound register is set in response to said completion bit being cleared.

23. (NEW) The apparatus according to claim 10, wherein (A) said processor means includes a direct memory access engine and said apparatus provides a delay when said direct memory access engine is not ready to present/receive said data to/from said memory means during a read/write operation, (B) said interface means comprises a control status register having a completion bit which indicates that said apparatus is ready to begin a new read/write operation, (C) said apparatus is ready to begin said new read/write operation to/from said memory means when said completion bit is cleared and (D) a direct memory access upper bound register is set in response to said completion bit being cleared.

24. (NEW) The method according to claim 11, wherein (A) said processor includes a direct memory access engine and said method provides a delay when said direct memory access engine is not ready to present/receive said data to/from said memory during

a read/write operation, (B) said interface circuit comprises a control status register having a completion bit which indicates that said method is ready to begin a new read/write operation, (C) said method is ready to begin said new read/write operation to/from said memory when said completion bit is cleared and (D) a direct memory access upper bound register is set in response to said completion bit being cleared.